Design of the Beam Shut-off Current Monitor Upgrade for the Advanced Photon Source*

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Abstract. Plans to eliminate the positron accumulator ring (PAR) from the Advanced Photon Source (APS) injector complex have created the need for a device to limit the allowable beam charge injected into the APS injector synchrotron. The beam shut-off current monitor (BESOCM) was chosen to provide this function. This new application of the BESOCM provided the opportunity to explore new design philosophies. Two design goals were to de-emphasize reliance on external signals and to become insensitive to timing variations. Both of these goals were accomplished by deriving the trigger directly from the beam. This paper will discuss the features of the new BESOCM design and present data demonstrating its function.

INTRODUCTION

The BESOCM system, in general, is designed to prevent excessive beam charge from being accelerated. The previous design is currently used in two locations, at the end of the APS linac and in the linac-to-PAR (LTP) transport line. Figure 1 shows their locations. Both the linac BESOCM [1] and the LTP BESOCM are used to limit the charge in a single macropulse to a specific level. If the level is exceeded, a set of relay contacts will be opened signaling the Access Control and Interlock System (ACIS) to interrupt generation of beam. These systems have been operational for more than six years and have demonstrated exceptional reliability.

Plans are underway to remove the positron accumulator ring (PAR) from operational use. When this occurs, electrons will be injected directly into the injector synchrotron from the APS linac, which means the LTP BESOCM will not be used during operations. Elimination of the PAR from operational use provided the opportunity to upgrade the BESOCM system. The goals of the new design were to become less susceptible to timing variations, decrease the sensitivity to one-time events, and make the verification process simpler.

The BESOCM upgrade was commissioned in August 1999. The system so far has only been used during direct injection studies. To date it has provided trouble-free performance.

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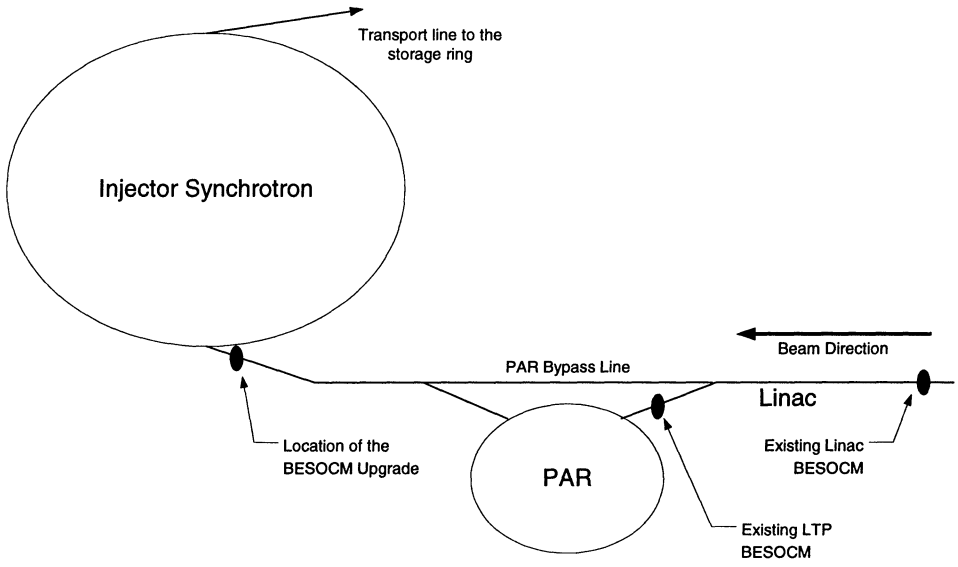

FIGURE 1. Partial APS accelerator machine layout showing the locations of the original BESOCMs as well as the location of the new upgraded BESOCM.

SYSTEM DESCRIPTION

The BESOCM system upgrade consists of an integrating current transformer (ICT) [2], three heliax® signal cables, and a chassis housing the processing electronics. The three cables include a signal cable from the transformer output, a signal cable for the system-generated self test, and a third cable for validation purposes. A block diagram of the system is shown in Figure 2.

The BESOCM system is designed to be fail-safe, meaning that if there is any failure related to the system, internally or externally, the BESOCM must command the ACIS control system to halt beam. The system must be redundant to the greatest extent possible. The system must detect and latch all failures [3] including the following:

- AC power is lost,
- The arm signals or trigger pulses are lost,
- The self test fails either the high or the low limit test,
- The magnitude of the measured beam charge exceeds the limit,
- The test winding opens or shorts, or the main winding opens or shorts.

The system is validated every six months. This process checks the trip levels by injecting a known pulse through the ICT and insuring a trip occurs when expected. The faults listed above are also induced for verification.

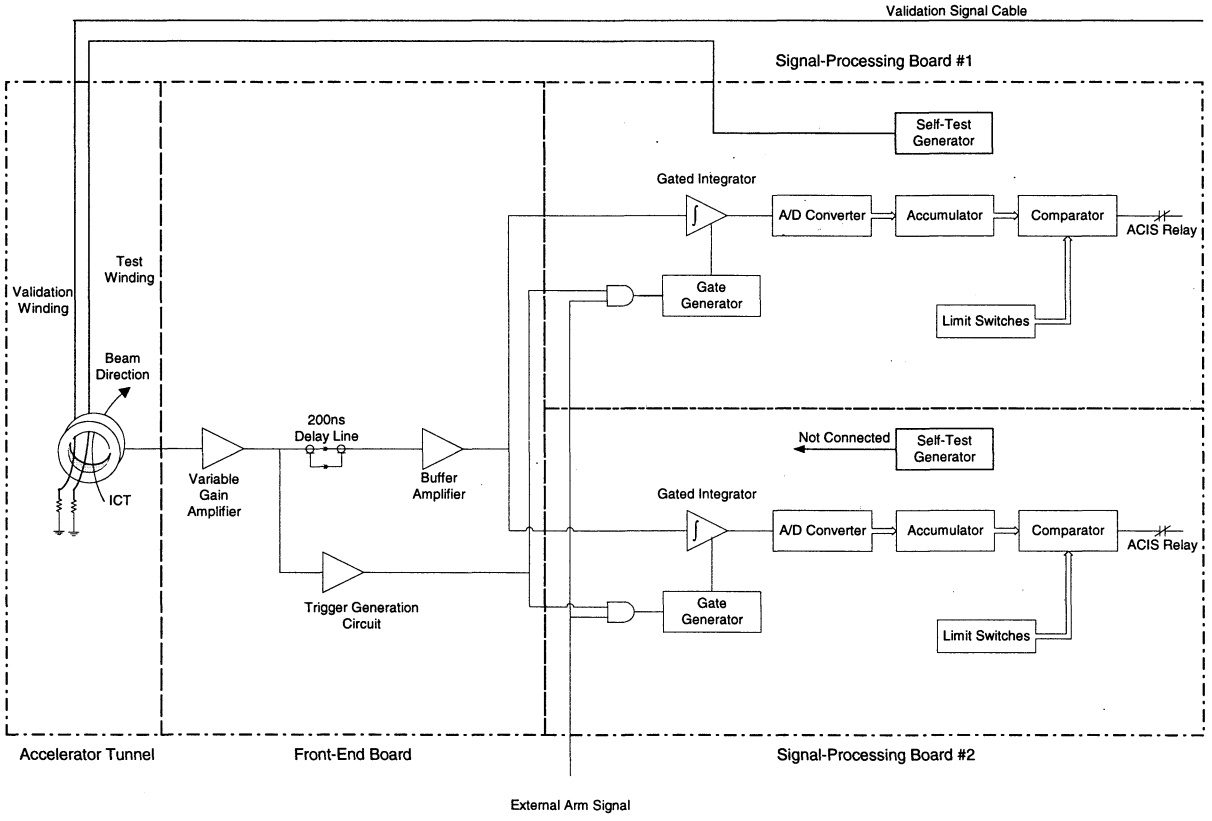

FIGURE 2. System block diagram showing the ICT, the front-end board, and the two signal-processing boards.

Three circuit boards reside in the BESOCM chassis. There is a front-end circuit board and two signal processing boards for redundancy. In normal operation, two pairs of normally open relay contacts per signal processing board are held in the closed position. This is done so that the relay contacts will open and trip the ACIS system if AC or DC power is lost. The BESOCM receives an arm signal from the timing system indicating the imminent arrival of a beam pulse. The arm signal is derived from the modulator trigger and is repetitive in nature. A beam pulse may or may not be generated for each modulator trigger. If a beam pulse is generated, it is guaranteed to arrive within 10 μs of the leading edge of the arm signal. There are watchdog timers on board that monitor both the arm signal from the timing system and the beam-derived trigger. With a properly functioning system, there will be at least one beam-derived trigger for each arm signal because the test pulse will cause a beam-derived trigger to be generated. If either the arm signal or the beam-derived trigger is missing for 1.5 seconds, this fault will be latched and the ACIS relay opened.

The arm signal can vary from 2 Hz to 30 Hz, and it is possible to have a beam pulse for each arm signal. Since the specification being enforced is a maximum of 20 nC at 2 Hz into the injector synchrotron, this implies the BESOCM must measure beam pulses ranging from 667 pC to 10 nC, a dynamic range of 23.5 dB.

Front-End Board

The front-end board provides signal conditioning, beam-derived trigger generation, and signal routing. The input signal originates from the ICT, installed just upstream of the injector synchrotron. This signal is buffered and provided to the front panel as a test point. A sketch of the front panel is shown in Figure 3. The signal is also routed to a variable gain stage. The gain can be set via dipswitches for flexibility in handling a variety of signal levels. Following amplification, the signal is routed to both a beam-derived trigger generation circuit and to an off-board, 200 ns analog delay. The delay is a neatly packaged length of 0.085" coaxial cable. This delay is sufficient to accommodate the propagation delay of the trigger generation circuit and a gate generation circuit found on the signal processing board. The delayed signal is brought back on board for further amplification and buffering. A buffered version of the trigger signal is provided to the front panel as a test point. Both the delayed signal and the detected trigger are now routed to redundant signal processing boards. The amplification serves two functions. It provides adequate signal for trigger generation, and it compensates for the losses in the delay line.

Signal-Processing Board

There are two independent signal-processing boards for redundancy. Identical in form and function, each board contains a gated integrator [4], a 12-bit analog-to-digital converter, a gate generation circuit, fault latches, a self-test generator, and a programmable logic device (PLD) for control and processing. Either of the signal-processing boards is capable of tripping the ACIS system. A block diagram of the signal processing section of this design is shown in Figure 4.

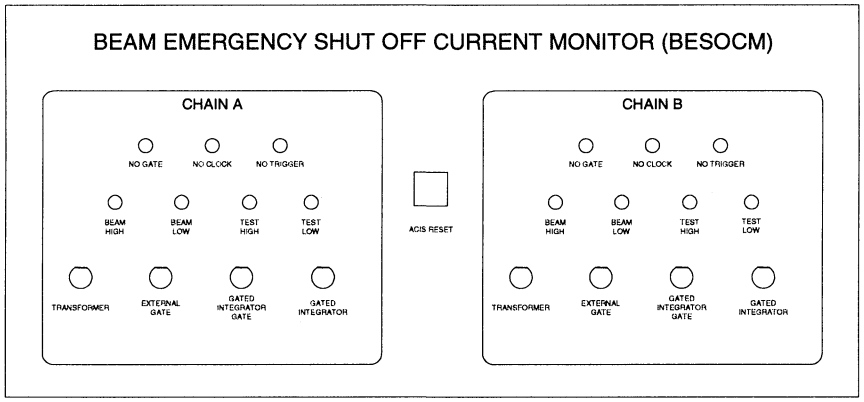

FIGURE 3. BESOCM chassis front panel.

For system troubleshooting, there are various signal test points and LED indicators that allow visual monitoring of a few selected faults. These are clock missing, arm signal missing, test pulse missing, as well as high or low beam faults and high or low test pulse faults. These or any of the other faults will open the ACIS relay.

The signal-processing board receives the delayed beam pulse and the beam-derived trigger from the front-end board as well as an arm signal from the timing system. When the chassis receives the arm signal from the timing system, the signal processing electronics wait up to 10 μs for the next beam-derived trigger to arrive. After this time has elapsed, any triggers received are rejected. This is done to prevent the system from processing false signals. The only exception is the trigger expected because of the test pulse, which is explained later. The beam-derived trigger generates a gate for the gated integrator. Both the gate delay and gate width are 8-bit programmable via dipswitches. A 12-bit analog-to-digital converter digitizes the gated integrator output. The result is accumulated for two seconds then compared to a trip limit. There are separate limits for positrons (e^+) and electrons (e^-). The limits are also programmable via dipswitches. Although positrons are no longer used at the APS, this feature was included for flexibility. If the accumulated signal exceeds the trip limit, a relay will open, notifying the ACIS system of the fault. Following the two-second accumulation, the accumulator is cleared and the process is repeated.

The signal processing board will produce a test pulse 65 μs after the arm signal. This pulse is sent to a test winding that passes through the ICT. The ICT output for this signal is processed by the same electronics as the real beam pulse up to the output of the ADC. A different circuit within the same PLD processes the test signal. Rather than accumulating over two seconds, as with the real beam, the test pulse is directly compared to the upper and lower limits. The test signal is used to verify the integrity of the system and therefore is checked against tight tolerances by a digital window detector. If the test pulse is not within the window, the ACIS relay is opened and the gun is disabled. The oscilloscope traces in Figure 5 and Figure 6 show the gate positioning for both the real beam pulse and the test pulse, respectively.

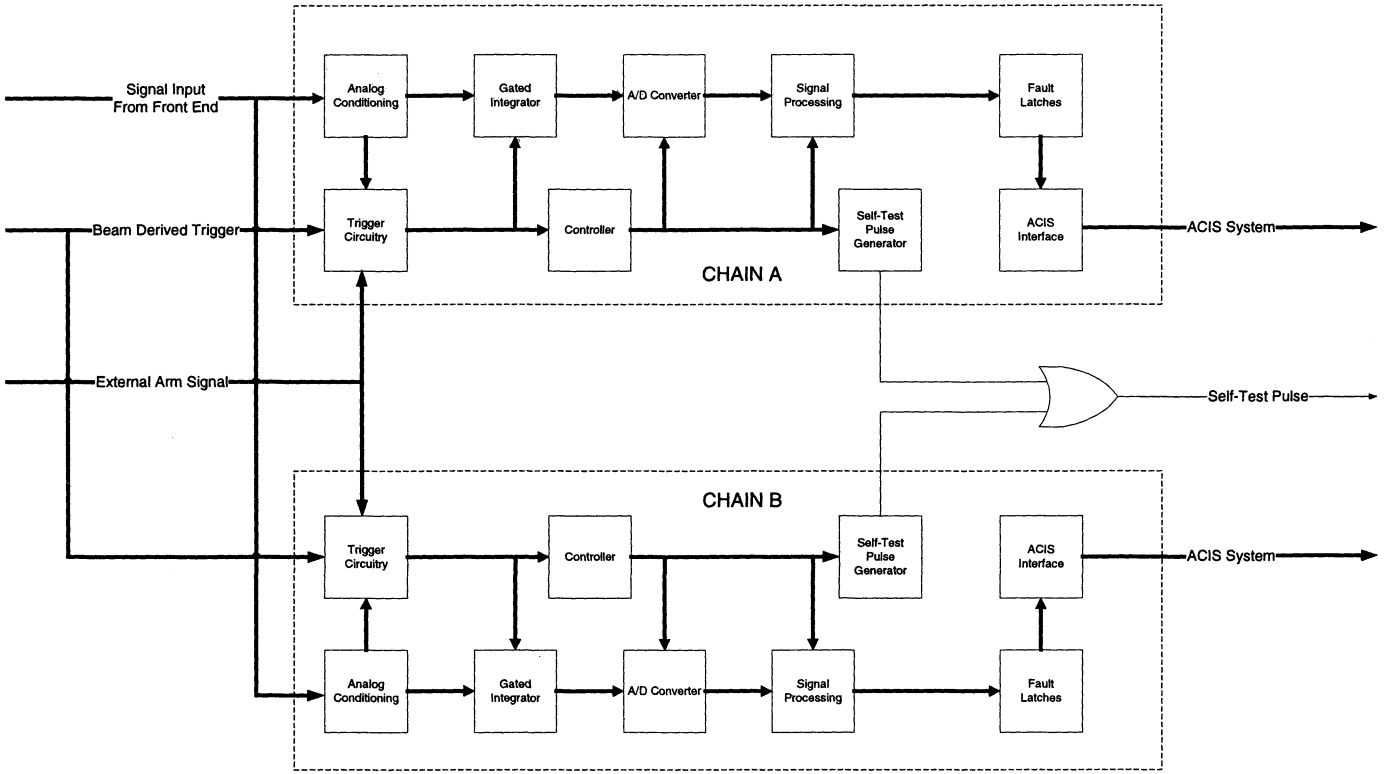

FIGURE 4. Block diagram of the signal-processing electronics.

Timing

Ensuring that timing uncertainty did not adversely impact the system was one of the primary design goals of this project. Timing uncertainty for this project is defined as the variation of the arrival time of the beam pulse relative to the arm signal. This timing relationship can be changed by varying the rf phase of the modulators. In the past, this uncertainty was handled by opening the integration gate early and keeping it open, such that the gate width would accommodate any of the possible timing scenarios. By deriving the trigger directly from the beam, the effect of this timing variation is minimized. Now the gate width can be made narrower, which reduces the chances of noise being introduced into the measurement.

The jitter of the gate signal relative to the arrival of the beam pulse was measured to be less than 0.8 ns.

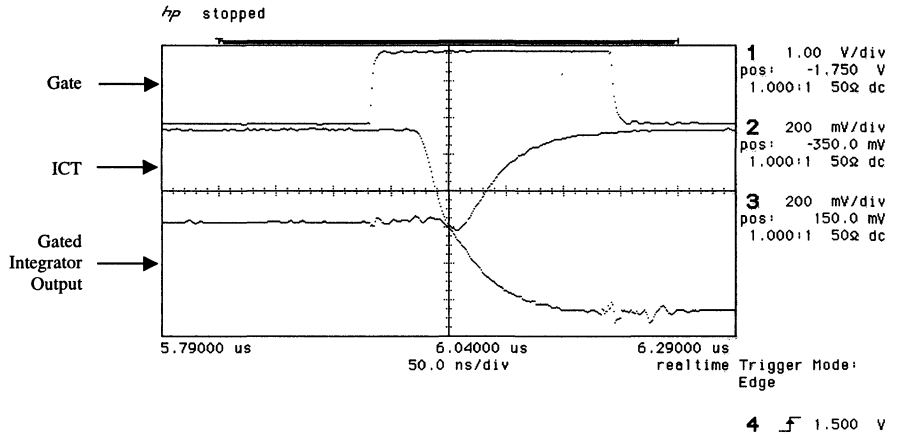

FIGURE 5. This oscilloscope trace shows the timing relationship between the gate signal, the delayed signal (real beam), and the gated integrator output.

FUTURE DEVELOPMENT

Plans for enhancements include providing all digital outputs to the rear panel for monitoring via the EPICS control system to enable remote observation of the system. There is already a remote reset available to the ACIS system but it is currently not used because the latched fault must be viewed physically prior to being cleared. Being able to view any faults remotely will potentially reduce the time necessary to re-establish normal operations.

The BESOCM upgrade is slated to replace the existing BESOCM units. The former system is predominately analog in nature and does not offer the benefit of a beam-derived trigger. The original BESOCM system also lacks the ability to accumulate several readings; as a result, it is susceptible to spurious trips.

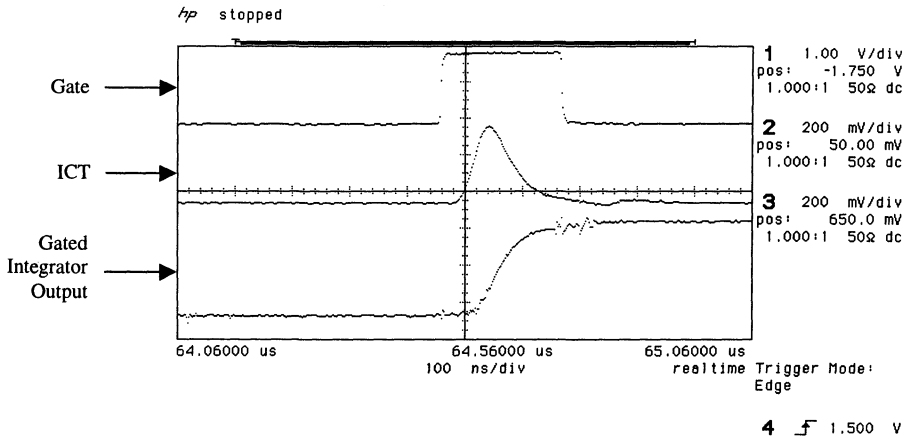

FIGURE 6. This oscilloscope trace shows the timing relationship between the gate signal, the delayed signal (test signal), and the gated integrator output.

CONCLUSION

Plans to remove the PAR from operational use have created the need for an additional safety device to limit the amount of charge injected into the APS injector synchrotron. An upgrade to the APS BESOCM was developed that improves upon the existing design by reducing the effects of external timing uncertainties and reducing the sensitivity to spurious events. This system has been validated and is used regularly during direct injection machine studies periods. When the PAR is decommissioned and direct injection is the operational standard for the APS, the BESOCM upgrade design discussed in this paper will enforce the safety limit imposed on the injector synchrotron.

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